Bounded Universal Droop Control to Enable the Operation of Power Inverters Under Some Abnormal Conditions and Maintain Voltage and Frequency Within Predetermined Ranges

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***Abstract*—The universal droop control (UDC) can be applied to power inverters having an impedance angle between $-\pi/2$ rad and $\pi/2$ rad to achieve voltage and frequency regulation and accurate proportional power sharing without the need of knowing the type or value of impedance. However, there is an increasing need for voltage and frequency regulation within predetermined ranges even under some abnormal conditions, such as overloading, sensor faults, and large set-point changes, etc. In this paper, a bounded nonlinear dynamics is introduced into the UDC to ensure that the voltage and frequency can always stay within predetermined ranges under normal and some abnormal conditions, up to hardware limits when current protection needs to be triggered. As a result, the proposed controller can extend the operational range of power inverters in terms of voltage and frequency regulation to cover different scenarios. More importantly, the ranges for both voltage and frequency can be chosen independently from each other. Since the original structure of the UDC is kept in the proposed controller, the properties of the UDC, such as without the need of knowing the type or value of impedance, are well maintained. The closed-loop stability of the system is established via the Lyapunov method. Extensive simulation and experimental results are presented to validate the effectiveness of the proposed controller.**

***Index Terms*—Droop control; Universal droop control (UDC); Bounded control; Bounded universal droop control (BUDC).**

I. Introduction

Nowadays, increasing distributed energy resources are integrated to the grid through power inverters. The power inverters should be controlled properly so that their integration does not jeopardize the stability and performance of power systems, and the controller design for power inverters has become one of major issues in the operation of power systems [1], [2].

Inspired by the response of the conventional synchronous generator to grid voltage and frequency variations, the droop control, which does not require any external communication mechanism among power inverters, has been adopted for power inverters to provide frequency and voltage regulation. The droop control framework represents an active area of research in terms of improving its dynamic performance using a virtual impedance [3], or eliminating the need for a dedicated synchronization unit [4], [5]. Recently, the droop control methodology has been adopted for AC microgrid [6], [7], DC microgrid [8], [9], solar power systems [10], [11] and wind power systems [12], [13]. However, the conventional droop control is sensitive to the output impedance type and value, affecting not only the power sharing accuracy but also the stability of the system. To overcome this limitation, a robust droop control strategy [14] is developed for power inverters to achieve accurate power sharing, as long as they have the same type of output impedance. In practice, there are different types of the output impedance for power inverters, which are inductive in most cases, but can be resistive, capacitive, resistive-inductive or resistive-capacitive. For inverters with different types of the output impedance, robust droop controllers have different forms. To find droop controllers that work for more general cases, some attempts have been proposed, such as a rotational transformation matrix to control the power angle in [15], a virtual complex impedance to redesign the power angle in [16], [17], and an adaptive neuro-fuzzy system to handle different impedance types in [18]. Furthermore, a universal droop control (UDC) principle has been developed without the need of knowing the impedance type in [19]. The UDC takes the form of the droop control principle for R-inverters, and it can be adopted to any inverters having an impedance angle between $-\pi/2$ rad and $\pi/2$ rad, to achieve tight frequency and voltage regulation.

As is well known, it is important to regulate the voltage within a predetermined range. For example, the ANSI C84.1 standard [20] specifies the steady-state operating voltage ranges for $120-600$ V systems within $\pm 5\%$ of the nominal voltage. If the voltage deviates too far above or below its predetermined value, it could potentially result in power loss in an area, and possible tripping of transmission lines and other elements [21]. At the same time, the reliable operation of the electric power system requires maintaining system frequency within predetermined ranges of the rated value as well. Frequency violation may result from changes in the balance between the generation and the load, e.g., the sudden loss of a large amount of load or a large generator. Possible consequences include under frequency load shedding, generation tripping, or cascading outages [22]. Thus, maintaining the voltage and frequency of power inverters within predetermined ranges is an essential requirement, in order to maintain system stability and to avoid potential damages. Although a saturation unit can be adopted to achieve the requirement, this often results in instability because of the integrator windup and the non-smooth control law response [23], [24]. In order to overcome this issue, many anti-windup designs are proposed [25], but with complex controller designs. Although adaptive droop control with online adaptation [26]–[28] can be adopted

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to achieve appropriate frequency and voltage regulation and avoid possible overloading, the bounded frequency and voltage regulation are not considered. In [29], a droop controller utilizing the transient droop characteristics is proposed to eliminate voltage amplitude and frequency deviations at the steady state. However, voltage and frequency violations may occur during the transient state, because the desired droop characteristics still influence the corresponding transient responses. A synchronverter is proposed in [30] to achieve bounded frequency and voltage regulation for safety purpose. However, the bounds for the voltage and frequency are not independently determined from each other as the bound for the voltage is dependent on the system frequency. Hence, there is a need to design a controller for the power inverter to ensure that the bounds for the voltage and frequency are independently chosen from each other. In [31], a bounded droop controller is introduced to guarantee the closed-loop stability and simultaneously to achieve the accurate load sharing. Motivated by [31], a bounded voltage control scheme is proposed for solar systems in [32], where the output voltage of solar systems can be regulated in a given range. However, the controllers in [31], [32] only guarantee the upper bound of output voltage, and the bounded frequency regulation is not considered.

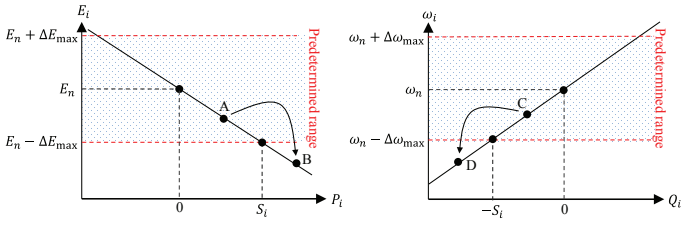
In this paper, a bounded universal droop control (BUDC) strategy for power inverters is developed, by adopting the bounded integral controller (BIC) [24], so that the frequency and voltage of inverters can be regulated within predetermined ranges under normal and some abnormal conditions, such as overloading, current sensor faults, and large set-point changes, etc., as long as the hardware current protection is not triggered. Since the BIC bounds the controller output through a bounded integral action, and there is no integral action in the frequency regulation loop of the UDC, the BIC cannot be directly applied to the UDC to achieve bounded frequency regulation. In order to solve this problem, the bounded nonlinear dynamics is re-designed, and the uncertainty and disturbance estimator (UDE) [33] is adopted to handle some coupled and uncertain terms caused by the designed bounded nonlinear dynamics. The contributions of this paper are highlighted as follows:

1) The BUDC is developed for power inverters to guarantee the voltage and the frequency stay within predetermined ranges during normal and some abnormal conditions.
2) The ranges for both voltage and frequency can be predetermined independently from each other.
3) The nonlinear dynamics is re-designed to achieve the bounded regulation, and the UDE technique is adopted to handle the coupled and uncertain terms caused by the designed nonlinear dynamics.
4) By using the Lyapunov method, the closed-loop stability, the bounded voltage and bounded frequency properties of inverters are analytically proven.

II. Problem Formulation and System Description

A. Problem Formulation

The UDC [19] provides a universal way to operate power inverters. It can work in the droop mode to participate in system



(a) (b)

Figure 1. Voltage and frequency violations from predetermined ranges. (a) Voltage droop. (b) Frequency droop.

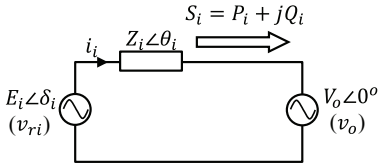


Figure 2. Power inverter delivering power to the grid

regulation, or the set mode to achieve accurate power delivery. The UDC generates a control signal $v_{ri} = \sqrt{2}E_i \sin(\omega_i t)$ with E_i being the root-mean-square (RMS) value of the voltage, and $\omega_i = 2\pi f_i$ being the angular frequency with the frequency f_i, generated from

$$\dot{E}_i = K_e\left(E_n - V_o\right) - n_i\left(P_i - P_{refi}\right) \quad (1)$$

$$\omega_i = \omega_n + m_i\left(Q_i - Q_{refi}\right) \quad (2)$$

where E_n is the rated voltage, ω_n is the rated angular frequency, V_o is the RMS value of AC voltage v_o, K_e is a positive control gain, n_i and m_i are droop coefficients, and P_{refi} and Q_{refi} are the reference values of the real power P_i and the reactive power Q_i, respectively. Although the UDC (1)-(2) takes the form of the droop control principle for power inverters with the resistive line impedance, it has been proven that it can be adopted to any inverters having an impedance angle between $-\pi/2$ rad and $\pi/2$ rad, which covers any practical L-, R-, C-, R_L- and R_C-inverters, to achieve tight frequency and voltage regulation [19]. Based on the guideline of the UDC [19], n_i and m_i are calculated as

$$n_i = \frac{\frac{\Delta E_{\max}}{E_n} K_e E_n}{S_i}, \quad m_i = \frac{\frac{\Delta\omega_{\max}}{\omega_n}\omega_n}{S_i} \quad (3)$$

where S_i is the rated capacity of the power inverter, $\frac{\Delta E_{\max}}{E_n}$ and $\frac{\Delta\omega_{\max}}{\omega_n}$ are the predetermined voltage and frequency regulation ratios for E_i and ω_i, respectively, at the rated power. The controllers (1)-(2) work for the droop mode but it can also work in the set mode by removing the term $K_e\left(E_n - V_o\right)$ from (1) and adding the integral term $\int m_i K\left(Q_i - Q_{refi}\right) dt$ into (2) with a positive control gain K.

During abnormal operations, the UDC cannot guarantee the voltage and frequency within predetermined ranges. For example, when the UDC is operated in the droop mode with $P_{refi} = 0$ and $Q_{refi} = 0$, the desired voltage and frequency droop curves are illustrated in Figs. 1(a) and (b), respectively. Under some abnormal conditions, voltage violations or frequency violations may occur, e.g., the voltage may move from Point A to Point B, as illustrated in Fig. 1(a), and the frequency may move from Point C to Point D, as illustrated in Fig. 1(b). Even for the set mode, similar violations may occur as well.

The objective of this paper is to develop a controller for power inverters, to make sure that, the RMS value of the output voltage E_i is maintained within a predetermined range around the rated voltage E_n, i.e.,

$$E_i \in (E_n - \Delta E_{\max},\, E_n + \Delta E_{\max}) \tag{4}$$

and the angular frequency ω_i is maintained within a predetermined range around the rated angular frequency ω_n, i.e.,

$$\omega_i \in (\omega_n - \Delta\omega_{\max},\, \omega_n + \Delta\omega_{\max}), \tag{5}$$

as long as the current protection is not triggered, which can be implemented easily by disabling the PWM signals if any current reaches its hardware limit.

B. Dynamics of Power Delivery

From (2), it can be seen that there is no integral action for the frequency regulation of the UDC, so the BIC method [24] cannot be directly applied to the UDC to achieve bounded frequency regulation and robust performance. Fig. 2 illustrates a power inverter $E_i\angle\delta_i$ delivering power to the grid $V_o\angle 0^o$ through an impedance $Z_i\angle\theta_i$, where δ_i is the phase difference between v_{ri} and v_o. The dynamics of the power delivery [1] can be re-designed and expressed as a first-order linear system plus a lumped uncertain term as

$$\dot{P}_i = \frac{V_o}{Z_n}u_{Ei} + \Delta_{pi} \tag{6}$$

$$\dot{Q}_i = -\frac{E_i V_o}{Z_n}u_{\omega i} + \Delta_{qi} \tag{7}$$

where

$$\begin{aligned}\Delta_{pi} =\ & \frac{E_i V_o(\omega_i-\omega_n)}{Z_i}\cos\delta_i\sin\theta_i + \frac{E_i\dot{V}_o}{Z_i}\cos\delta_i\cos\theta_i \\ & + \frac{E_i\dot{V}_o}{Z_i}\sin\delta_i\sin\theta_i - \frac{E_i V_o(\omega_i-\omega_n)}{Z_i}\sin\delta_i\cos\theta_i \\ & + \frac{V_o\dot{E}_i}{Z_i}\sin\delta_i\sin\theta_i + \frac{V_o\dot{E}_i}{Z_i}\cos\delta_i\cos\theta_i - \frac{V_o}{Z_n}\dot{E}_i \\ & - \frac{2V_o\dot{V}_o}{Z_i}\cos\theta_i + \frac{V_o}{Z_n}\left(\dot{E}_i - u_{Ei}\right)\end{aligned} \tag{8}$$

$$\begin{aligned}\Delta_{qi} =\ & -\frac{E_i V_o(\omega_i-\omega_n)}{Z_i}\sin\delta_i\sin\theta_i - \frac{E_i\dot{V}_o}{Z_i}\sin\delta_i\cos\theta_i \\ & + \frac{E_i\dot{V}_o}{Z_i}\cos\delta_i\sin\theta_i - \frac{E_i V_o(\omega_i-\omega_n)}{Z_i}\cos\delta_i\cos\theta_i \\ & + \frac{E_i V_o}{Z_n}(\omega_i-\omega_n) - \frac{V_o\dot{E}_i}{Z_i}\sin\delta_i\cos\theta_i - \frac{2V_o\dot{V}_o}{Z_i}\sin\theta_i \\ & + \frac{V_o\dot{E}_i}{Z_i}\cos\delta_i\sin\theta_i - \frac{E_i V_o}{Z_n}\left[(\omega_i-\omega_n) - u_{\omega i}\right]\end{aligned} \tag{9}$$

represent the lumped uncertain terms, Z_n is the nominal impedance, and u_{Ei} and $u_{\omega i}$ are control laws to be designed to handle the terms Δ_{pi} and Δ_{qi}.

III. Bounded Universal Droop Control

A. Bounded Voltage Controller

Define the tracking error for the real power as

$$e_{pi} = P_{refi} - P_i \tag{10}$$

with the desired error dynamics designed as

$$\dot{e}_{pi} = -k_{pi}E_{qi}e_{pi} \tag{11}$$

where k_{pi} is a positive control gain, and E_{qi} will be designed later to dynamically introduce the bounded voltage property. Substituting (6) into the desired error dynamics (11) results in

$$u_{Ei} = \frac{Z_n}{V_o}\left(\dot{P}_{refi} - \Delta_{pi} + k_{pi}E_{qi}e_{pi}\right). \tag{12}$$

According to the dynamics (6), Δ_{pi} can be represented as

$$\Delta_{pi} = \dot{P}_i - \frac{V_o}{Z_n}u_{Ei} \tag{13}$$

which indicates that the term Δ_{pi} can be obtained from the controller u_{Ei} and the known dynamics. Then, the UDE design procedure provided in [33] is adopted to estimate Δ_{pi} as

$$\hat{\Delta}_{pi} = L^{-1}\left\{G_{pfi}(s)\right\} * \left(\dot{P}_i - \frac{V_o}{Z_n}u_{Ei}\right) \tag{14}$$

where L^{-1} means the inverse Laplace transformation, $*$ is the convolution operator, and $G_{pfi}(s)$ is a strictly-proper stable filter. Replacing Δ_{pi} with $\hat{\Delta}_{pi}$ in (12), the UDE-based control u_{Ei} can be formulated as

$$\begin{aligned}u_{Ei} =\ & \frac{Z_n}{V_o}[L^{-1}\left\{\frac{1}{1-G_{pfi}(s)}\right\} * \left(\dot{P}_{refi} + k_{pi}E_{qi}e_{pi}\right) \\ & - L^{-1}\left\{\frac{sG_{pfi}(s)}{1-G_{pfi}(s)}\right\} * P_i].\end{aligned} \tag{15}$$

Although the controller u_{Ei} is designed to handle the uncertain term, the voltage may exceed the predetermined range. The BIC in [24] is then introduced to regulate the final voltage controller output E_i into the predetermined range around the rated value, i.e., $E_i \in (E_n - \Delta E_{\max}, E_n + \Delta E_{\max})$. The bounded voltage controller is proposed as

$$\begin{aligned}\dot{E}_i =\ & -c_{p1}(E_i - E_n)\left[\frac{(E_i-E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2 - 1\right] \\ & + c_{p2}E_{qi}^2 u_{Ei}\end{aligned} \tag{16}$$

$$\begin{aligned}\dot{E}_{qi} =\ & -c_{p1}E_{qi}\left[\frac{(E_i-E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2 - 1\right] \\ & - \frac{c_{p2}(E_i-E_n)E_{qi}u_{Ei}}{\Delta E_{\max}^2}\end{aligned} \tag{17}$$

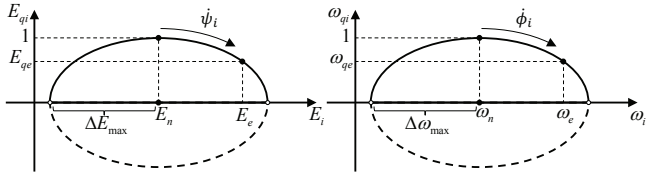
where the initial control states are chosen as $E_i(0) = E_n$ and $E_{qi}(0) = 1$; c_{p1} and c_{p2} are positive control gains. The behavior of the bounded voltage controller can be discussed as follows. Consider the following Lyapunov function candidate

$$W_{pi} = \frac{(E_i-E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2. \tag{18}$$

Its time derivative, after substituting (16)-(17) is

$$\dot{W}_{pi} = -2c_{p1}\left[\frac{(E_i-E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2 - 1\right]\times\left[\frac{(E_i-E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2\right]. \tag{19}$$

Since the initial conditions satisfy $E_i(0) = E_n$ and



(a) (b)

Figure 3. Variables E_i, E_{qi} and ω_i, ω_{qi} on the $E_i - E_{qi}$ and $\omega_i - \omega_{qi}$ planes, respectively.

$E_{qi}(0) = 1$, there is $\dot{W}_{pi}(0) = 0$ and thus

$$W_{pi}(t) = W_{pi}(0) = \frac{[E_i(0) - E_n]^2}{\Delta E_{\max}^2} + E_{qi}^2(0) = 1,\ t \geq 0. \tag{20}$$

Both E_i and E_{qi} will start and stay thereafter on the ellipse

$$W_{Ei} = \left\{ E_i,\ E_{qi} \in \mathbb{R} :\ \frac{(E_i - E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2 = 1 \right\} \tag{21}$$

as shown in Fig. 3(a). The behavior of the bounded voltage controller can be understood further by defining the transformation $E_i = E_n + \Delta E_{\max} \sin\psi_i$ and $E_{qi} = \cos\psi_i$. Note that the term $\frac{(E_i - E_n)^2}{\Delta E_{\max}^2} + E_{qi}^2 - 1$ is zero on the ellipse W_{Ei}. Then by taking into account (16), after some calculations, there is

$$\dot{\psi}_i = \frac{c_{p2} E_{qi}}{\Delta E_{\max}} u_{Ei} \tag{22}$$

which means that E_i and E_{qi} travel on the ellipse W_{Ei} with the angular velocity $\dot{\psi}_i$, as shown in Fig. 3(a). Based on (22), the bounded voltage controller can settle down at the steady state when $u_{Ei} = 0$. That is to say, both E_i and E_{qi} can converge to the desired equilibrium values E_e and E_{qe} with the angular velocity $\dot{\psi}_i$, respectively, as shown in Fig. 3(a).

Since the initial conditions satisfy $E_i(0) = E_n$ and $E_{qi}(0) = 1$, and the angular velocity $\dot{\psi}_i$ depends on E_{qi} from (22), both E_i and E_{qi} only travel on the upper semiellipse of W_{Ei}. If $E_{qi} \to 0$, it holds $\dot{\psi}_i \to 0$, and then the controller will slow down and remain on the upper semiellipse of W_{Ei}, avoiding oscillations on the ellipse W_{Ei}. Since E_i travels on the upper semiellipse W_{Ei} for all the time, the voltage is bounded, i.e., $E_i \in (E_n - \Delta E_{\max},\ E_n + \Delta E_{\max})$.

The proposed voltage controller has two parts: a bounded nonlinear dynamics part (16)-(17) to introduce the bounded voltage property, and a UDE-based controller part (15) to handle the nonlinearities and uncertainties, as illustrated in upper part of Fig. 4. From the controller (15), the reference P_{refi} is needed. When the power inverter is required to achieve the accurate real power delivery, P_{refi} can be determined according to user requirements, hardware capabilities, or performance requirements. When the power inverter is required to operate in the droop mode, P_{refi} is determined according to the droop function (1). Thus, P_{refi} can be expressed as

$$P_{refi} = P_{seti} \cdot \mathrm{SW} + \frac{K_e\,(E_n - V_o)}{n_i} \cdot (1 - \mathrm{SW}) \tag{23}$$

where P_{seti} is the set-point value of the real power, and SW is a digital switch defined as

$$\mathrm{SW} = \begin{cases} 0 & \text{droop mode} \\ 1 & \text{set mode} \end{cases} \tag{24}$$

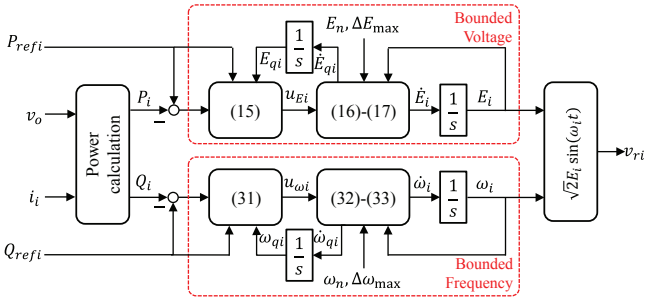


Figure 4. Implementation of the proposed BUDC

In other words, the proposed bounded voltage controller can be operated in the droop mode or the set mode.

B. Bounded Frequency Controller

Similarly, a UDE-based frequency controller in conjunction with a bounded frequency controller can be designed. Define the tracking error for the reactive power as

$$e_{qi} = Q_{refi} - Q_i \tag{25}$$

with the desired error dynamics designed as

$$\dot{e}_{qi} = -k_{qi}\omega_{qi}e_{qi} \tag{26}$$

where k_{qi} is a positive control gain, and ω_{qi} will be designed later to dynamically introduce the bounded frequency property. Substituting (7) into the desired error dynamics (26) results in

$$u_{\omega i} = -\frac{Z_n}{E_i V_o}\left(\dot{Q}_{refi} - \Delta_{qi} + k_{qi}\omega_{qi}e_{qi}\right). \tag{27}$$

According to the dynamics of power delivery (7), Δ_{qi} can be represented as

$$\Delta_{qi} = \dot{Q}_i + \frac{E_i V_o}{Z_n} u_{\omega i} \tag{28}$$

which indicates that the uncertain term Δ_{qi} can be obtained from the control signal $u_{\omega i}$ and the known dynamics. Following the UDE design procedure, Δ_{qi} can be estimated as

$$\hat{\Delta}_{qi} = L^{-1}\{G_{qfi}(s)\} * \left(\dot{Q}_i + \frac{E_i V_o}{Z_n} u_{\omega i}\right) \tag{29}$$

with a strictly-proper stable filter $G_{qfi}(s)$. Replacing Δ_{qi} with $\hat{\Delta}_{qi}$ in (27), it yields

$$\begin{aligned} u_{\omega i} = & -\frac{Z_n}{E_i V_o}[L^{-1}\left\{\frac{1}{1 - G_{qfi}(s)}\right\} * \left(\dot{Q}_{refi} + k_{qi}\omega_{qi}e_{qi}\right) \\ & - L^{-1}\left\{\frac{sG_{qfi}(s)}{1 - G_{qfi}(s)}\right\} * Q_i]. \end{aligned} \tag{30}$$

To achieve the frequency droop function, the digital switch SW defined in (24) is used into the controller $u_{\omega i}$, and then the UDE-based frequency controller is formulated as

$$\begin{aligned} u_{\omega i} = & -\frac{Z_n}{E_i V_o}[L^{-1}\left\{\frac{1}{1 - G_{qfi}(s)}\right\} * \left(\dot{Q}_{refi} + k_{qi}\omega_{qi}e_{qi}\right) \\ & - L^{-1}\left\{\frac{sG_{qfi}(s)}{1 - G_{qfi}(s)}\right\} * Q_i] \cdot \mathrm{SW} \\ & + [\omega_n + m_i\,(Q_i - Q_{refi})] \cdot (1 - \mathrm{SW}). \end{aligned} \tag{31}$$

When SW is set as 0, the controller $u_{\omega i}$ achieves the droop function given in (2). When SW is set as 1, the controller works in the set mode. Similarly, the following bounded frequency controller can be introduced to regulate the final frequency controller output ω_i into the predetermined range around the rated value, i.e., $\omega_i \in (\omega_n - \Delta\omega_{\max}, \omega_n + \Delta\omega_{\max})$. The bounded frequency controller is proposed as

$$\begin{aligned}\dot{\omega}_i &= -c_{q1}(\omega_i - \omega_n)\left[\frac{(\omega_i-\omega_n)^2}{\Delta\omega_{\max}^2} + \omega_{qi}^2 - 1\right] \\ &\quad -c_{q2}\omega_{qi}^2(\omega_i - u_{\omega i}) \qquad (32)\\ \dot{\omega}_{qi} &= -c_{q1}\omega_{qi}\left[\frac{(\omega_i-\omega_n)^2}{\Delta\omega_{\max}^2} + \omega_{qi}^2 - 1\right] \\ &\quad + \frac{c_{q2}(\omega_i-\omega_n)\omega_{qi}}{\Delta\omega_{\max}^2}(\omega_i - u_{\omega i}) \qquad (33)\end{aligned}$$

where the initial control states are chosen as $\omega_i(0) = \omega_n$, $\omega_{qi}(0) = 1$; c_{q1} and c_{q2} are positive constant gains. Similarly, the behavior of the bounded frequency controller can be understood. Consider the following Lyapunov function candidate

$$W_{qi} = \frac{(\omega_i-\omega_n)^2}{\Delta\omega_{\max}^2} + \omega_{qi}^2. \qquad (34)$$

Substituting (32)-(33) into the time derivative of W_{qi} shows that, the angular frequency ω_i and the variable ω_{qi} will start and stay on the ellipse

$$W_{\omega i} = \left\{\omega_i,\, \omega_{qi} \in \mathbb{R} :\ \frac{(\omega_i-\omega_n)^2}{\Delta\omega_{\max}^2} + \omega_{qi}^2 = 1\right\} \qquad (35)$$

with the angular velocity

$$\dot{\phi}_i = -\frac{c_{q2}\omega_{qi}(\omega_i - u_{\omega i})}{\Delta\omega_{\max}} \qquad (36)$$

as shown in Fig. 3(b). Both ω_i and ω_{qi} can converge to the desired equilibrium values ω_e and ω_{qe} with the angular velocity $\dot{\phi}_i$, respectively. If the initial conditions satisfy $\omega_i(0) = \omega_n$ and $\omega_{qi}(0) = 1$, both ω_i and ω_{qi} are restricted only on the upper semiellipse of $W_{\omega i}$. If $\omega_{qi} \to 0$, then $\dot{\phi}_i \to 0$ as well, so that the oscillation on the ellipse $W_{\omega i}$ can be avoided. Since ω_i travels on the upper semiellipse $W_{\omega i}$ for all the time, it holds true that $\omega_i \in (\omega_n - \Delta\omega_{\max},\, \omega_n + \Delta\omega_{\max})$.

The proposed frequency controller can be implemented as illustrated in the lower part of Fig. 4.

C. Closed-Loop Stability

Replacing Δ_{pi} with $\hat{\Delta}_{pi}$ in (12), and Δ_{qi} with $\hat{\Delta}_{qi}$ in (27), there are

$$u_{Ei} = \frac{Z_n}{V_o}\left(\dot{P}_{refi} + k_{pi}E_{qi}e_{pi} - \hat{\Delta}_{pi}\right) \qquad (37)$$

$$u_{\omega i} = -\frac{Z_n}{E_i V_o}\left(\dot{Q}_{refi} + k_{qi}\omega_{qi}e_{qi} - \hat{\Delta}_{qi}\right). \qquad (38)$$

Consider the Lyapunov function candidate $V = \frac{1}{2}e_{pi}^2 + \frac{1}{2}e_{qi}^2$. Its time derivative along with (6), (7), (10), (25), (37), and (38), after some calculations, yields

$$\dot{V} = -k_{pi}E_{qi}e_{pi}^2 - k_{qi}\omega_{qi}e_{qi}^2 + e_{pi}\tilde{\Delta}_{pi} + e_{qi}\tilde{\Delta}_{qi} \qquad (39)$$

where $\tilde{\Delta}_{pi} = \hat{\Delta}_{pi} - \Delta_{pi}$ and $\tilde{\Delta}_{qi} = \hat{\Delta}_{qi} - \Delta_{qi}$. By applying Young's inequality with a positive constant ε, i.e., $e_{pi}\tilde{\Delta}_{pi} \le \frac{\varepsilon}{2}e_{pi}^2 + \frac{1}{2\varepsilon}\tilde{\Delta}_{pi}^2$ and $e_{qi}\tilde{\Delta}_{qi} \le \frac{\varepsilon}{2}e_{qi}^2 + \frac{1}{2\varepsilon}\tilde{\Delta}_{qi}^2$, to (39), it results in

$$\begin{aligned}\dot{V} &\le -\left(k_{pi}E_{qi} - \frac{\varepsilon}{2}\right)e_{pi}^2 - \left(k_{qi}\omega_{qi} - \frac{\varepsilon}{2}\right)e_{qi}^2 \\ &\quad + \frac{1}{2\varepsilon}\tilde{\Delta}_{pi}^2 + \frac{1}{2\varepsilon}\tilde{\Delta}_{qi}^2 \\ &\le -\rho V + c \qquad (40)\end{aligned}$$

where $\rho = 2\min\left\{\min(E_{qi})k_{pi} - \frac{\varepsilon}{2},\, \min(\omega_{qi})k_{qi} - \frac{\varepsilon}{2}\right\}$ and c is an upper bound of $\frac{1}{2\varepsilon}\tilde{\Delta}_{pi}^2 + \frac{1}{2\varepsilon}\tilde{\Delta}_{qi}^2$. In Section III.A and III.B, it has been proven that both E_{qi} and ω_{qi} only travel on the upper part of W_{Ei} and $W_{\omega i}$, respectively, so that $\min(E_{qi}) > 0$ and $\min(\omega_{qi}) > 0$. Given any positive parameters k_{pi} and k_{qi}, there always exists a positive constant ε such that $\rho > 0$. Thus, solving (40) gives $0 \le V(t) \le \frac{c}{\rho}(1 - e^{-\rho t}) + V(0)e^{-\rho t}$, where $V(0) = \frac{1}{2}e_{pi}^2(0) + \frac{1}{2}e_{qi}^2(0)$ is the initial value. Thus, $V(t)$ is bounded for all $t \ge 0$, and e_{pi} and e_{qi} are bounded for all $t \ge 0$ as well. Together with the fact that $\dot{P}_{refi}$ and $\dot{Q}_{refi}$ are bounded, the UDE-based control parts (15) and (31) are bounded as well. Besides, it has been proven that for any initial conditions, the control parts (16)-(17) and (32)-(33) introduce an ultimate bound [24]. Hence, all control signals are bounded. With e_{pi} and e_{qi} bounded, it can be concluded that all closed-loop signals are bounded. In other words, the system is in principle stable but in practice care still needs to be taken in order to meet the requirement of performance and to avoid instability caused by discretization etc.

IV. Experimental Studies

A test rig, as shown in Fig. 5(a), was built up for experimental validation. The circuit diagram is shown in Fig. 5(b) with the parameters summarized in Table I. The system includes two power inverters, two DC sources, and an oscilloscope. Here, two SYNDEM Smart Grid Research and Educational Kits [34] were adopted and configured as single-phase inverters. The experimental results were collected and recorded with the oscilloscope through on-board digital-to-analog converter (DAC) channels, without the need of using isolated probes.

The goal is to achieve bounded voltage and frequency regulations, e.g., with voltage variations within $\pm 5\%$ around the rated voltage 110 V and frequency variations within $\pm 0.5\%$ around the rated angular frequency $2\pi \times 60$ rad/s, i.e., $\Delta E_{\max} = 5\% \times E_n$ and $\Delta\omega_{\max} = 0.5\% \times \omega_n$. The droop coefficients are calculated accordingly as: $n_1 = 5\% \times E_n \times K_e/S_1 = 0.11$ and $m_1 = 0.5\% \times \omega_n/S_1 = 0.00628$; $n_2 = 2n_1$ and $m_2 = 2m_1$. Hence, it is expected that $P_1 = 2P_2$ and $Q_1 = 2Q_2$.

Additionally, the proposed controller can be designed to achieve other goals, e.g. to improve the output voltage quality of power inverters. In general, there exist harmonics in the voltage of a power inverter. There are two sources of harmonics: one is from the power inverter because of the PWM and the switching, and the other is from loads or the grid. In order to improve the transient response and reduce voltage harmonics, the filter of the UDE-based control is selected as

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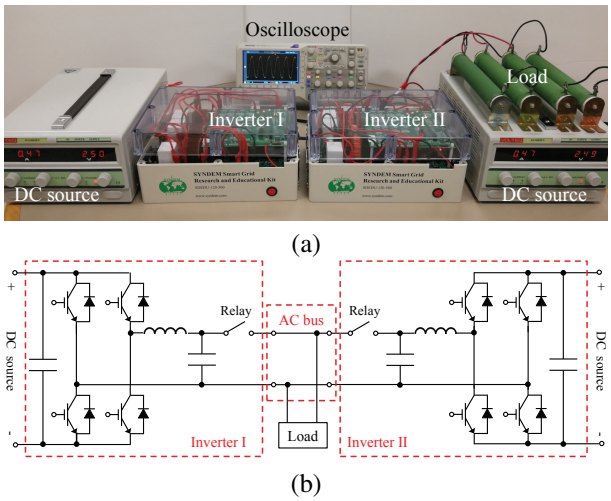

Figure 5. Experimental test rig. (a) Setup. (b) Circuit diagram.

Table I
SYSTEM PARAMETERS AND CONTROL PARAMETERS

Parameters	Values	Parameters	Values
AC voltage (RMS)	110 V	E_n	110 V
AC frequency	$2\pi \times 60$ rad/s	ω_n	$2\pi \times 60$ rad/s
DC source voltage	250 V	$\Delta E_{\max}$	$5\% \times 110$ V
S_1, S_2	300 VA	$\Delta\omega_{\max}$	$0.5\% \times 2\pi \times 60$ rad/s
K_e	6	K	0.0214
n_1	0.11	m_1	0.00628
n_2	0.11×2	m_2	0.00628×2
c_{p1}	1	c_{q1}	0.5
c_{p2}	5	c_{q2}	1
k_{p1}, k_{p2}	20	k_{q1}, k_{q2}	20
τ_p	0.05	τ_q	0.01
ξ	0.01	h	3

Note: The rated phase current is 5A but the power capacity of 300 VA is used.

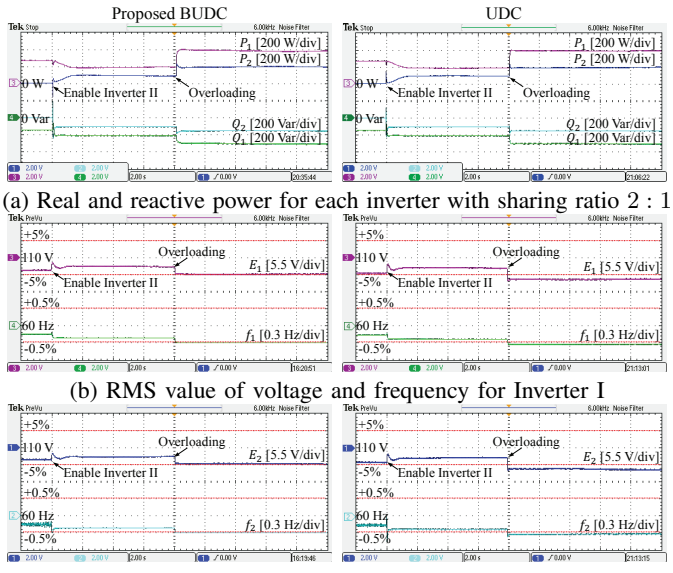

Figure 6. Experimental results for Case 1: Overloading (Left: Proposed BUDC; Right: Original UDC [19]).

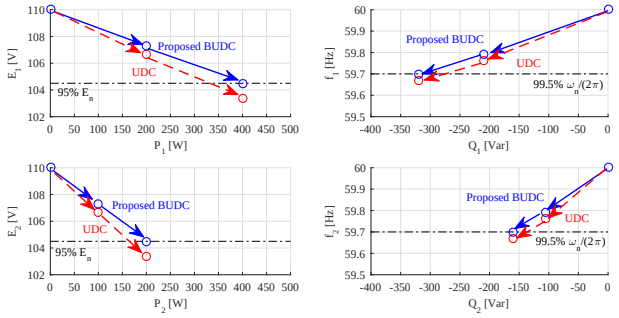

Figure 7. Operational points on the $P_i - E_i$ and $Q_i - f_i$ planes in Case 1. (a) Measured voltage. (b) Measured frequency.

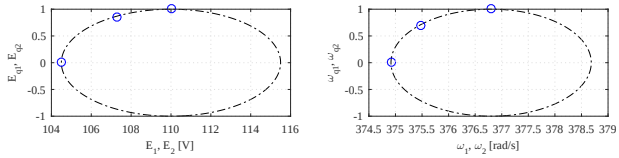

Figure 8. Operational points on the $E_i - E_{qi}$ and $\omega_i - \omega_{qi}$ planes in Case 1. (a) Measured voltage. (b) Measured frequency.

$$G_{pf1}(s) = G_{pf2}(s) = 1 - \left(1 - \frac{1}{\tau_p s + 1}\right)\left(1 - \frac{2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}\right) \quad (41)$$

$$G_{qf1}(s) = G_{qf2}(s) = 1 - \left(1 - \frac{1}{\tau_q s + 1}\right)\left(1 - \frac{2\xi h\omega s}{s^2 + 2\xi h\omega s + (h\omega)^2}\right) \quad (42)$$

The first-order filters $\frac{1}{\tau_p s+1}$ and $\frac{1}{\tau_q s+1}$ are used to handle step responses or step disturbances, and the resonant filter $\frac{2\xi h\omega s}{s^2+2\xi h\omega s+(h\omega)^2}$ is to handle the voltage harmonics with $h = 3$ to reduce the third voltage harmonics. Based on the guideline of UDE control framework [33], the filter parameters τ_p and τ_q should be selected small with the unity gain and zero phase shift over the spectrum of the uncertainty. However, in practice, due to the hardware limitation, the filter parameters cannot be chosen too small, because a filter with a too wide bandwidth requires high computational power, which may increase the cost. Thus, how to select the filter parameter also depends on the hardware capability and performance requirements.

Other control parameters are summarized in Table I. Since the power inverter itself is with inductive output impedance, in order to evaluate the proposed method under various conditions, and to reduce the cost and the power loss, the idea of the virtual impedance concept [14], [35] is adopted to configure two power inverters with different types and values of the output line impedance. Inverter I is configured to have 0.04 p.u. inductive impedance and Inverter II is configured to have 0.07 p.u. resistive impedance.

To validate the proposed BUDC, several experiments were carried out under different scenarios, e.g. with overloading (Case 1), AC current sensor fault (Case 2), and large set-point change (Case 3), all in comparison with the original UDC [19]. Moreover, further comparison with the UDC with a saturation

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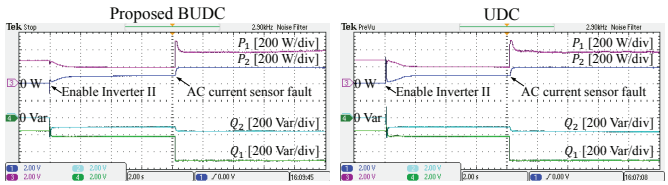
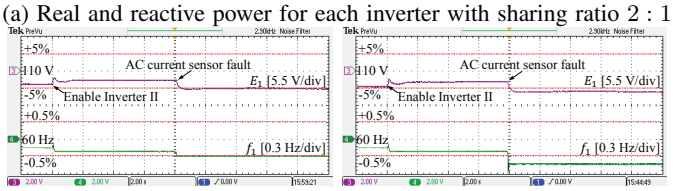
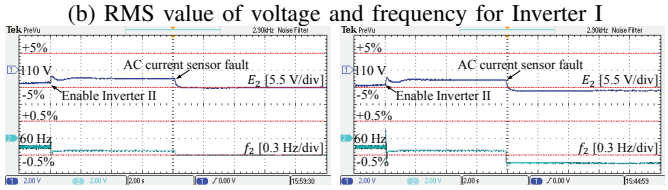


(a) Real and reactive power for each inverter with sharing ratio 2 : 1



(b) RMS value of voltage and frequency for Inverter I



(c) RMS value of voltage and frequency for Inverter II

Figure 9. Experimental results for Case 2: AC current sensor fault (Left: Proposed BUDC; Right: Original UDC [19]).

unit, the UDC with the tracking anti-windup method [36], and another droop control strategy without amplitude or frequency deviation [29] were also implemented (Case 4).

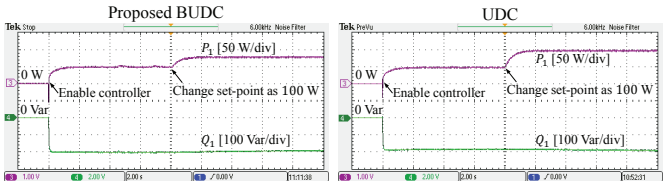
A. Case 1: Overloading

In this case, the abnormal condition with real and reactive power overloading is considered to test the performance under the droop mode. A resistor and a capacitor are connected to the AC bus to cause both real and reactive power overloading. The results are shown in Figs. 6-8.

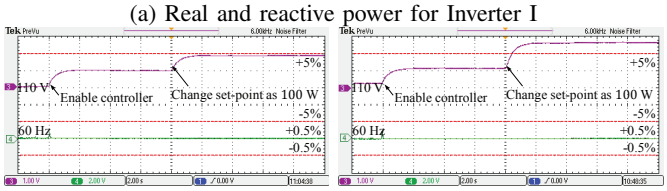
Initially a 40 Ω resistor was connected to the AC bus as the load with Inverter I operated in the droop mode. At $t = 2$s, Inverter II was enabled and connected to the AC bus. The two inverters shared the load properly, with the real and reactive power about $P_1 = 200$ W, $P_2 = 100$ W and $Q_1 = -210$ Var, $Q_2 = -105$ Var, respectively. The negative reactive power was due to the capacitor in the LC filter and the 40 μF capacitor as part of the load. The real and reactive power is less than the rated capacity of inverter $S = 300$ VA. Both the voltage and frequency of two inverters were regulated within the predetermined ranges for both the proposed BUDC and the UDC, as shown in Fig. 6(b) and (c).

Then, at $t = 10$s, a 40 Ω resistor and a 45 μF capacitor were connected to the AC bus, which caused the abnormal condition with real and reactive power overloading. The two inverters shared the load properly, at about $P_1 = 400$ W, $P_2 = 200$ W and $Q_1 = -320$ Var, $Q_2 = -160$ Var. Inverter voltage and frequency violations occurred for the UDC but not for the proposed BUDC. As can be seen from Fig. 6(b) and (c), both inverter voltages E_1 and E_2 were regulated at about 103.4 V, and inverter frequencies f_1 and f_2 were regulated at about 59.67 Hz for the UDC, which is out of the predetermined range, but the inverter voltage and frequency can be regulated within the predetermined range for the proposed BUDC.

The steady-state operational points of this case are summarized in Fig. 7 with the measured voltage and frequency. The



(a) Real and reactive power for Inverter I



(b) RMS value of voltage and frequency for Inverter I

Figure 10. Experimental results for Case 3: Large set-point change of Inverter I with Inverter II operated in the droop mode (Left: Proposed BUDC; Right: Original UDC [19]).

voltage and frequency violations occurred to the UDC but not to the proposed BUDC. The operational points on the $E_i - E_{qi}$ and $\omega_i - \omega_{qi}$ planes are given in Fig. 8, which illustrates the bounded voltage and frequency properties.

This function is important for inverters to ride through overload up to a certain level while maintaining the frequency and voltage within predetermined ranges. If the overload exceeds the specified level, then current protection should be triggered.

B. Case 2: AC Current Sensor Fault

In this case, the abnormal condition with an AC current sensor fault is considered with two inverters operated in parallel. The experimental results are given in Fig. 9. Initially, Inverter I was operated in the droop mode with a 40 Ω resistor. At $t = 2$s, Inverter II was enabled and connected to the AC bus. The two power inverters shared the real and reactive power well, at about $P_1 = 200$ W, $P_2 = 100$ W, and $Q_1 = -210$ Var, $Q_2 = -105$ Var, respectively. Both inverter voltages and frequencies were well regulated in the predetermined ranges. The voltage was at about 107.3 V for the proposed BUDC and at about 106.7 V for the UDC, and the frequency was at about 59.79 Hz for both the proposed BUDC and the UDC, as shown in Fig. 9(b) and (c). Then, at $t = 10$s, a fault was assumed at the current sensor of Inverter I. The measured current became 5 times its actual value, which resulted in an abnormal operation and caused the real and reactive power to increase, as shown in Fig. 9(a). In this case, proportional power sharing is not maintained as expected. As shown in Fig. 9(b) and (c), inverter voltage and frequency were regulated within the predetermined ranges for the proposed BUDC. However, the voltage and frequency violations occurred for the UDC, at about 103.4 V for the inverter voltage and 59.58 Hz for the frequency.

C. Case 3: Large Set-Point Change

Another abnormal condition, i.e., with a large set-point change, is considered to validate the proposed BUDC at the set mode. In this case, Inverter II was operated in the droop mode to simulate the grid operation, and Inverter I was operated in

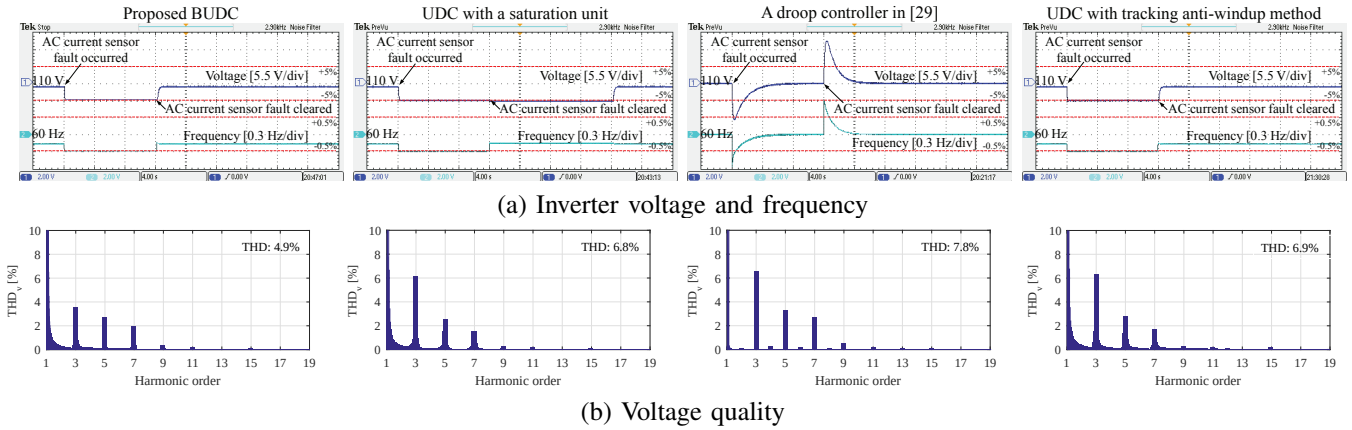


Figure 11. Experimental results for Case 4: Comparison with other methods.

the set mode to deliver power to the grid. Fig. 10 illustrates the experimental results. From Fig. 10(a), after the system was enabled at $t = 2$s with $P_{ref1} = P_{set1} = 50$ W and $Q_{ref1} = -200$ Var, both P_1 and Q_1 converged to the reference values 50 W and -200 Var, respectively. From Fig. 10(b), the voltage and the frequency were well regulated in the predetermined ranges by both the proposed BUDC and the UDC, delivering similar performance in the set mode under normal condition. Then, at $t = 10$s, the set-point value of the real power was changed to 100 W. As shown in Fig. 10(a), the proposed BUDC regulated the real power P to 80 W, below its set-point value 100 W, because the voltage reached and settled at its upper bound, $105\% \times 110$ V. However, for the UDC, the voltage reached about 117.2 V, as shown in Fig. 10(b), which violated the upper bound, although the real power P reached its set-point value 100 W, as shown in Fig. 10(a).

D. Case 4: Comparison with Other Methods

To further demonstrate the advantage of the proposed BUDC, its performance was compared with some other control methods, including the UDC with a saturation unit, the droop controller proposed in [29], and the UDC with the tracking anti-windup method [36].

In this case, an inverter connected to a diode rectifier load was adopted to carry out the experiments. An AC current sensor fault was introduced during the tests. The droop coefficients for the four control methods are the same for fair comparison. The experimental results are given in Fig. 11.

At $t = 0$s, the inverter was started to work properly. At $t = 4$s, a fault was assumed at the current sensor with the measured current becoming 10 times its actual value. For the UDC with the saturation unit, although both the voltage and frequency were maintained within the predetermined ranges, as shown in the second column of Fig. 11(a), the saturation unit caused an apparent integrator windup, and was displayed as a horizontal line when $t \in [16, 32]$s. Besides, at $t = 16$s, after the AC current sensor fault was cleared, the UDC with a saturation unit was not able to regulate the voltage until about $t = 32$s due to the integrator windup.

As for the droop controller proposed in [29], as shown in the third column of Fig. 11(a), it can be observed that, after the AC current sensor fault was occurred/cleared, although the voltage and frequency deviations were eliminated at the steady state, the transient performance was not satisfactory.

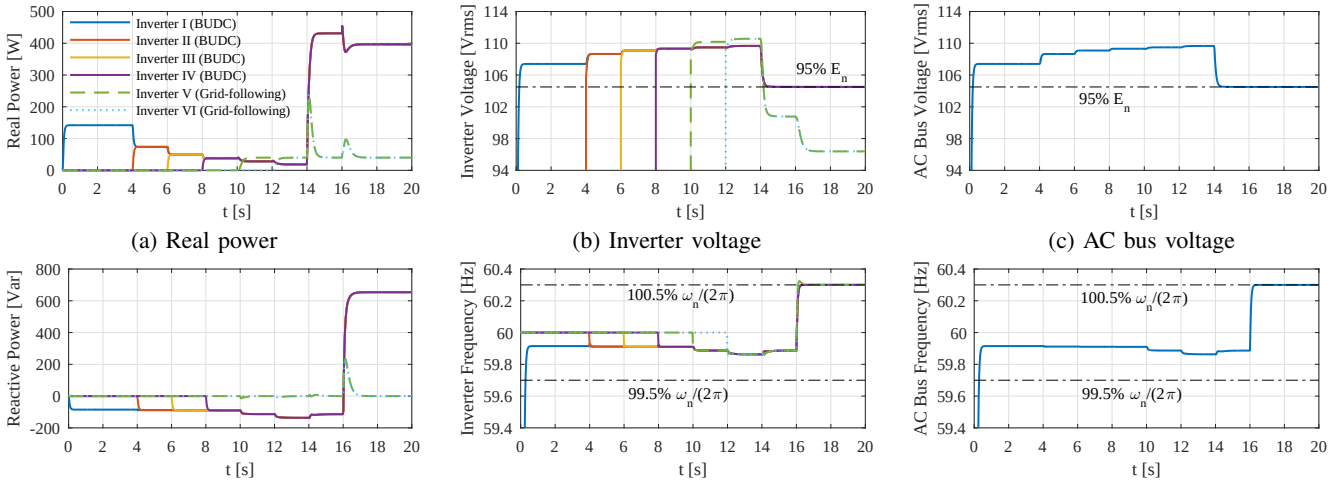
As for the UDC with the tracking anti-windup method, shown in the fourth column of Fig. 11(a), it can achieve similar performance for the voltage and frequency regulation as the proposed BUDC, because the tracking anti-windup method can effectively handle the integrator windup.

In order to demonstrate the flexibility and merits of the proposed controller, the voltage THD of the four cases are shown in Fig. 11(b). The UDC with a saturation unit, the droop controller proposed in [29], and the UDC with the tracking anti-windup method cannot handle voltage harmonics properly but, by adopting the UDE filter (41)-(42) in the proposed controller, the third voltage harmonics is reduced to 3.6%; and the THD value is reduced to 4.9%, which meets the standard requirement of harmonic voltage limits based on the IEEE STD 519 (<5%), as shown in Fig. 11(b).

V. Simulation Studies to Validate the Operation of BUDC Inverters with Grid-following Inverters

To further demonstrate the merits of the proposed BUDC, a simulation platform with six power inverters was built in MATLAB/Simulink/SimPowerSystems. Power inverter I, II, III and IV were equipped with the proposed BUDC with the power sharing ratio 1 : 1 : 1 : 1, while Inverter V and VI were equipped with the current-controlled method [1] as grid-following inverters with the real power references set at 40 W. In this scenario, the filter is selected as the first-order low-pass filter with parameters τ_p and τ_q shown in Table I. The rest control parameters, system parameters and the control goal are the same as those in the experimental studies. The simulation results are given in Fig. 12.

Before $t = 4$s, Inverter I was enabled and connected to the AC bus with an initial resistive load 80 Ω. The real power for Inverter I was about 150 W, as shown in Fig. 12(a), and the reactive power was about -100 Var, as shown in Fig. 12(d). Then, the other five inverters, including three inverters equipped with the proposed BUDC and two grid-following inverters, were connected to the AC bus every 2 seconds. Since the real power and reactive power were less than the rated capacity, the inverter voltage, inverter frequency, AC bus voltage and frequency were well regulated within the predetermined ranges, as shown in Fig. 12.



(a) Real power (b) Inverter voltage (c) AC bus voltage

(d) Reactive power (e) Inverter frequency (f) AC bus frequency

Figure 12. Simulation results validating the operation of mixed BUDC inverters and grid-following inverters with real and reactive power overloading.

At $t = 14$s, a 6 Ω resistor was connected to the AC bus, causing the abnormal condition of real power overloading. As shown in Fig. 12(a), the real power for Inverter I, II, III and IV was about 440 W, which was larger than the rated capacity of the inverters, but the inverter voltages were well regulated within the predetermined range, as shown in Fig. 12(b). For Inverter V and VI, the real power was regulated at the set-points after some transients, as shown in Fig. 12(a), but voltage violations occurred, as shown in Fig. 12(b). The AC bus voltage was well regulated within the predetermined range, as shown in Fig. 12(c), indicating that the proposed BUDC was capable of regulating the overall voltage of the system even when grid-following inverters were not able to.

At $t = 16$s, an 8 mH inductor was connected to the AC bus, causing another abnormal condition with reactive power overloading. According to Fig. 12(d), the reactive power consumption was about 650 Var for Inverter I, II, III and IV, which was larger than the rated capacity, but the frequencies of Inverter I, II, III and IV and the frequency of the AC bus were maintained within the predetermined range, as shown in Fig. 12(e) and (f). As grid-following inverters, Inverters V and VI followed the AC bus frequency well.

As a result, the proposed BUDC maintained the AC bus voltage and frequency within predetermined ranges under abnormal conditions of overloading even when some inverters were not capable of regulating the voltage and frequency.

VI. Conclusion

A BUDC strategy has been developed for power inverters to make sure that, the voltage and frequency can be regulated within predetermined ranges even under some abnormal conditions, such as real power and reactive power overloading, AC current sensor faults, and large set-point changes. This helps extend the operational range of power inverters up to the physical limit of inverters when current protection should be triggered. At the core of the BUDC, bounded nonlinear dynamics has been designed for the voltage loop and the frequency loop to provide bounded voltage and frequency properties, and the UDE-based control technique has been embedded into the proposed BUDC to handle uncertainties introduced in modeling the system. Moreover, it has been shown that the design flexibility of the proposed controller can be explored to improve voltage quality. Experimental and simulation studies have been carried out to validate the performance of the proposed BUDC.

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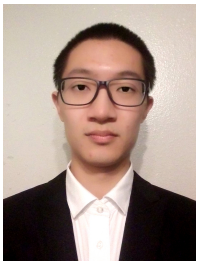

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